Amendments to the Specification:

Please replace paragraph [0012] with the following amended paragraph:

[0012] Figure 8 illustrates one embodiment of the invention showing staged switching; ~~and~~

Please replace paragraph [0013] with the following amended paragraph:

[0013] Figure 9 illustrates one embodiment of the invention controlling the transistors which are directly tied to an output; and

Please add the following new paragraph after paragraph [0013]:

[0013.1] Figure 10A, Figure 10B, and Figure 10C illustrate embodiments of the present invention.

Please add the following new paragraph after paragraph [0037]:

[0037.1] Figure 10A, Figure 10B, and Figure 10C illustrate embodiments of the present invention. In Figure 10A at 1002 an output signal is generated. At 1004 the output signal that was generated is received. At 1006 a signal is fed back based on the received output signal to at least one transistor in a stacked output transistor array having two or more transistors. In Figure 10B at 1012 an output signal is generated. At 1014 the output signal that was generated is received. At 1016 a signal is fed back based on the received output signal to at least one transistor in a stacked output

transistor array having two or more transistors after passing the output signal through a device selected from the group consisting of a resistor, a capacitor, a n type transistor, and a p type transistor. In Figure 10C at 1022 an output signal is generated. At 1024 the output signal that was generated is received. At 1026 a signal is fed back based on the received output signal to at least one transistor in a stacked output transistor array having two or more transistors after comparing the received output signal to a reference voltage and passing the output signal through a device selected from the group consisting of a resistor, a capacitor, a n type transistor, and a p type transistor.